DELTA TELEMETRY SYSTEMS

DATA ACQUISITION

Data Transmission Test Set w/ Bert

MODEL 650

KEY FEATURES

- 1 bps to 36 Mbps Operation (Standard)
  1 bps to 50 Mbps Operation*
- Independent Transmitter and Receiver
- Measures: Bits, Seconds, Bits in Error, Seconds in Error, Bit Error Rate (instantaneous and average)
- Data Symmetry & Bit Slip Tests
- TX & RX Frequency Measurement
- 16 PRN Sequence Codes Forward & Reverse 2n-1, n= 5, 7, 9, 11, 15, 20, 23, 31 (Forward or Reverse) and User Defined Taps on 31-bit Register
- Fixed Programmable Data Patterns 8, 16, 32, 64, 128, 256-bit or Dotting
- Internal DDS Frequency Synthesizer
  IRIG Code Generation & Conversion
- Randomizer / Derandomizer (Fwd & Rev)
- IRIG (215-1), 29-1, 211-1, 217-1, 223-1, V.35, V.36

* Optional

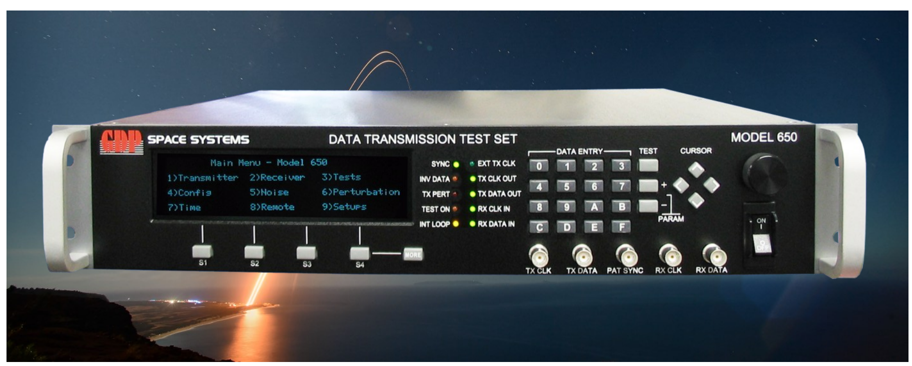
GENERAL DESCRIPTION

The GDP Model 650 is an affordable, versatile solution for data link verification and qualification. Independent transmit and receive paths allow rapid fault isolation and end-to-end link analysis. Programmable signal perturbations include noise, baseline offset, missing bits, jitter, and signal level variation. Built-in features such as a 6-digit frequency synthesizer and IRIG code generator/converter make it ideal for PCM telemetry test and evaluation.

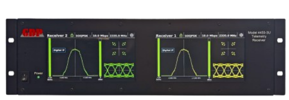
Measurement capabilities include accumulated bit errors, BER, elapsed test time, errored seconds, errors per second, error symmetry, bit slips, and measured Tx/Rx clock rates. The microprocessor control augments high-speed hardware to enhance flexibility.

A modular architecture supports a programmable frequency range from 1 bps to 50 Mbps. IRIG input/output and a robust BER module enable comprehensive testing via front panel or remote control. All high-speed functions run in hardware, with lower-speed tasks handled by embedded processing.

The Model 650 supports data link and Bit Sync testing for ground stations or satellite data systems. Loop-back testing, noise injection, and GDP VI Software integration make it a powerful tool for evaluating telemetry links from the antenna through the bit synchronizer. Bit synchronizer performance in noise and jitter can be measured and curves plotted at the push of a button. These curves can be saved for future reference. Additional functions like Acquisition time and Link Delay measurement are also available.



RELATED PRODUCTS

Antenna	Receiver	Bit Sync	Gateway
			

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DATA ACQUISITION

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TECHNICAL SPECIFICATIONS

Operation:

Independent Transmitter and Receiver

- 1 bps to 36 Mbps NRZ codes Standard
- (17.5 Mbps for 2X codes) Standard
- 1 bps to 50 Mbps NRZ codes Optional
- (30 Mbps for 2X codes) Optional

TTL-50 Mbps, Bipolar-40 Mbps, RS-422-40 Mbps

Frequency Display: · Receive and Transmit Bit Rate, Measured

Input Termination:

High Z / Low-Z on TTL & Bipolar

Data Pattern Selectable:

Forward and Reverse PRN codes:

2 5-1, 2 7-1, 29-1, 211-1, 215-1, 217-1, 219-1, 220-1, 221-1, 223-1, 225-1, 231-1, User selectable Taps

Recycle data patterns, programmable:

8, 16, 24, 32, 64, 128, 256 bits or Dotting pattern

IRIG Bit-Codes: ·NRZ-L/M/S; BiØ-L/M/S; DM-M/S

Data Randomizer / Derandomizer:

V.35, V.36 or Fwd/Rev RNRZ-L 2N-1(N=15 [IRIG-STD 106], 9, 11, 17, 23)

Convolutional Encoder (Viterbi):

Rate ½ ; K 7

Selectable convolution order and polarity

TRANSMITTER

Data/Clock Outputs:

Transmit Data

Transmit Clock

Clock Input:

External Transmit Clock - Selectable

Transmit Timing:

Internal Frequency Synthesizer

Six (6) digit-plus-exponent

Data Perturbations:

Force output ALL 1s or ALL 0s

Insert a single error

Insert a single slip

Insert bit-error-rates from 1.0E-06 to 0.5

Insert Gap

Selectable data slip up to 9999 bit times

Selectable data gap up to 9999 bit times

Bit Rate Jitter (Option)

AC Base-line Variation (w/ Analog Option)

Signal Amplitude Modulation (w/ Analog Option)

RECEIVER

Receive Data and Clock, Synchronization:

Auto Polarity Correction

Auto-correlation BER up to 3 x 10 -1.

ReSynch Threshold, Selectable

Error Allowance Threshold

Tests:

Test length from 102 thru 1012 bits

Total Count since test start: Bits, Bits-in-Error, Seconds, Errored-Seconds, Slips

Calculations: ·Bit-Error Rate, Symmetry, Average Bit-Error Rate

Sync Acquisition (Option)

Data Link Delay (Option)

BER vs Eb/No Performance

Jitter Performance

ANALOG INTERFACE (OPTION)

Transmit Data with level and offset adjust:

Signal level: 100 mVp-p to 4 Vp-p (50 Ω Load)

DC offset: Up to +5V or - 5V (Peak signal + Offset + Noise)

AC Offset

Bit Rate Jitter

Noise: (Option)

Internal programmable Eb/No generator

External Noise Input

LOCAL FRONT PANEL CONTROL

Power ON/OFF

Display and Keypad

Soft Control Keys

LED Status and Test Points

MISCELLANEOUS

AC Input:

90 to 264 VAC Auto-set

Single Phase, 47-63 Hz

Size:

3.5 (H) x 20 (D) x 17 (W), inches

Weight: 20 lbs

Mounting: 19 inch EIA rack mount

Environment, Operating:

Temperature: 0 to 40o C

Relative Humidity: 5 to 95%, no condensation

Altitude: 0 to 10,000 ft

Forced-air Cooling

REMOTE CONTROL

Ethernet - 10/100 Base T (Std)

RS-232 Serial Interface (Std)

Recognizing that no standard product fits every mission, Delta Telemetry Systems is ready to deliver tailored solutions for your unique application requirements.

Specifications subject to change without notice.

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